

# High Density Plasma Flood System for Wafer Charge Neutralisation

Hiroyuki Ito<sup>a</sup>, Hiroshi Asechi<sup>a</sup>, Yasuhiko Matsunaga<sup>a</sup>, Masahiko Niwayama<sup>b</sup>,  
Kenji Yoneda<sup>b</sup>, Michael Vella<sup>c</sup>, Mike Reilly<sup>c</sup> and Walt Hacker<sup>c</sup>

<sup>a</sup>Applied Materials Japan, Narita, Chiba 286-0825, Japan

<sup>b</sup>ULSI Process Technology Development Center, Matsushita Electronics Corp.

<sup>c</sup>Electro-Graph, Carlsbad, CA 92009, USA

hiro\_ito@amat.com

**Abstract** - Plasma Flood System, a low energy electron generator, has been widely used as an effective tool to neutralise wafer charging induced by ion implantation. Although it has been successful in achieving the full device yield under high current ion implantation, further advancement in device design imposed a need to minimise the wafer charging down to a few volts due to the use of thin gate oxide of less than 10nm thickness.

High Density Plasma Flood System (HD PFS) was thus developed for the Applied Materials xR series Ion Implanters to maintain the maximum throughput with high current processes without compromising on device yield. HD PFS is a high efficiency charge neutraliser that supplies very low energy (<3eV) electrons at high emission (>300mA). The system has a unique configuration of magnetic circuit and arc discharge profile that enables the effective transport of electrons from the plasma source to the wafer while reducing the power consumption by one order of magnitude. This paper discusses the structure and the performance of the HD PFS in terms of electron transport efficiency and energy distribution. Typical operation window is also shown by using the yield of MOS capacitor devices at different gate oxide thickness (3.5, 5 and 10nm). Six months of filament life has been demonstrated.

## . INTRODUCTION

Charge neutralisation of wafers during ion implantation has been one of the most important tasks for controlling implant processes [1-3]. Methods to achieve the neutralisation have also gone through a series of evolution due to a need to reduce the energy of compensatory charges, i.e. electrons, as gate oxides become thinner [4].

Dense plasma source technique, such as Plasma Flood System (PFS) of Applied Materials [4], is now widely used to maintain good yield for thin gate oxide devices. Although it has been successful in achieving the task, there is still a need to improve the neutralisation performance in order to maximise the process throughput with increased beam current and very thin gate oxide (thickness less than 10nm). This means that the electron energy must be reduced and the electron flux must be increased.

High Density Plasma Flood System (HD PFS) has thus been developed for the Applied Materials xR series Ion Implanters in order to satisfy the new requirement. HD PFS is an improved version of the existing PFS which generates low energy electrons by using a unique “accel/decel” method [4]. The configuration of the source head has been largely changed, which resulted in very compact hardware and high transport efficiency of electrons. Combined with the redesigned “Guide Tube”, the system offers the complete neutralisation of positive charging due to ion beam, while the risk of negative charging is minimised. Optimisation of arc efficiency also made the life time of filament exceptionally long (over 6 months). The same design concept is adopted to a PFS for AMAT PI9000, 9200 and 9500 systems [5].

This paper describes the design and the performance of the HD PFS in terms of charging characterisation and the test device results using CHARM [6] and MOS capacitors.

### . HD PFS - Design and Operation

#### A. Design

The schematic view of the HD PFS is shown in Fig.1. The source head was largely changed from the previous PFS model [4] in its shape and mounting. This means the improvement in arc efficiency and electron transport by optimising the magnetic field profile and the plasma coupling. The system uses a proven accel/decel operation to generate low energy electrons by grounding the filament and the Guide Tube that transports the electrons with a aid of plasma confinement by magnetic cusp field and negative bias potential [4].

The compact design (40mm in width) allowed the system to be fitted in very small room where the charge neutralisation is required. Control electronics and software are basically identical to those of the existing PFS.

It should also be noted that the line of sight to the filament is completely eliminated, therefore, tungsten contamination on wafer surface is almost undetectable.

Due to the major improvement in electron transport efficiency, typical arc current required to maintain high enough electron emission is now reduced by one order of magnitude. Arc current of as low as 0.5A is normally sufficient to perform 20mA high dose implant. Low arc operation enabled the filament to last for more than 6 months.

#### B. Operation

Except for the use of lower arc current, the method to operate the HD PFS is the same as that of the previous PFS. Primary parameter to control the electron emission is arc current. Net flux of electrons to the wafer can be controlled by arc current and/or Guide Tube potential.

The function of the HD PFS can be well depicted by recording a few monitoring parameters as described below.

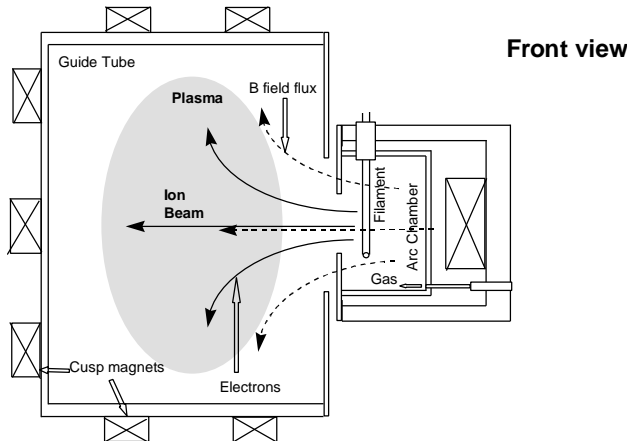


Fig.1 Schematic view of the HD PFS. Plasma in the arc chamber is coupled onto the beam plasma inside the Guide Tube near the wafer.

1) Emission Current : Emission currents at 30V of arc are plotted against arc current in Fig.2 at tube bias voltage of 0V. Argon gas was used as a source feed material. Emission current of HD PFS (150mA at 1A of arc) is higher than Previous PFS (10mA at 1A of arc) by one order of magnitude. This allows HD PFS to use very low arc operation (arc current below 1A).

2) Wheel Current : Wheel currents are plotted in Fig.3. With HD PFS, positive reading on wheel current disappears at 0.5A of arc current. On the other hand, previous PFS hardly made the wheel current negative with high current implantation, indicating that the positive charging always remains.

3) Charge Voltage on capacitively coupled charge sensor : Charge voltages on 5000Å sheet oxide wafer are plotted in Fig.4. HD PFS controlled the voltage below 0V at low arc current (0.5A). Previous PFS was not able to eliminate positive charging (>10V) even at maximum arc current (6A), indicating a risk of positive charging damage.

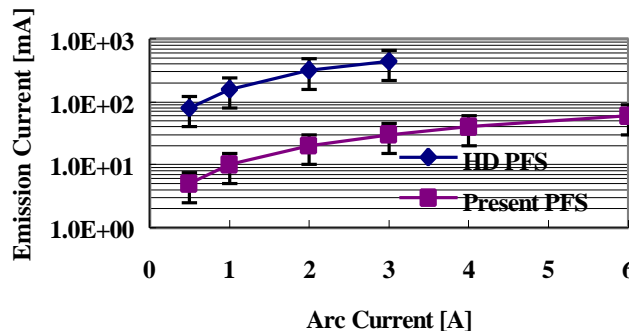


Fig.2 Emission Current in accel/decel mode is plotted against arc current at 0V of tube with As<sup>+</sup>/50keV/20mA.

4) Operation window : It has been known experimentally that the operation window to give a good device yield tends to be between +5 and -15V on Charge Sensor reading. HD PFS showed the good operation window between 0.5A to

3A of arc current for the high current beam, whereas the previous PFS showed a narrow window towards the maximum arc current.

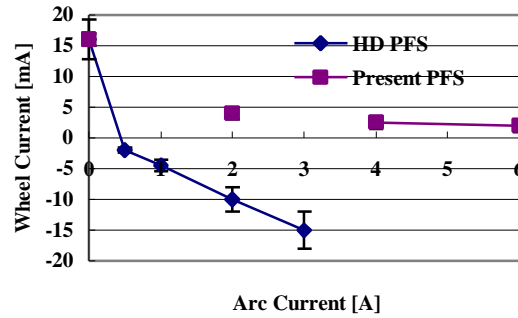


Fig.3. Wheel Current in accel/decel mode is plotted against arc current at 0V of tube with As<sup>+</sup>/50keV/20mA

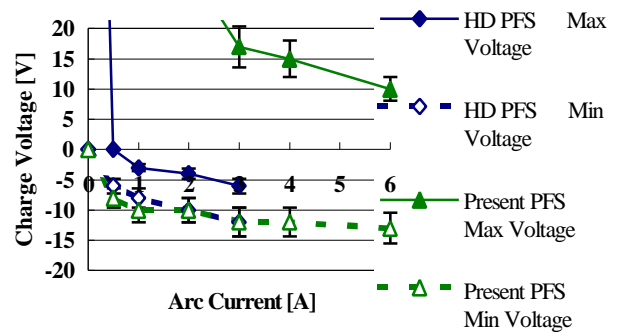


Fig.4. Charge Voltage in accel/decel mode is plotted against arc current at 0V of tube with As<sup>+</sup>/50keV/20mA

### C. Tungsten Emission from PFS

Level of tungsten on wafer surface in conjunction with PFS operation was evaluated with SIMS by using As<sup>+</sup>/80keV/20mA/5E15 cm<sup>-2</sup> Implant.

Measured level of tungsten from the HD PFS was about 5E9cm<sup>-2</sup> which is roughly the same as the detection limit of the measurement. Tungsten emission was proven to be minimised due to the low arc current (i.e. low filament current) operation and the complete elimination of the line of sight to filament.

## . PERFORMANCE on TEST DEVICES

Charge neutralisation performance of HD PFS was evaluated by using a series of charge sensitive MOS capacitors with different gate oxide thickness and EEPROM.

### A. Antenna MOS capacitors

Yield results of antenna MOS capacitors with thin gate oxide (less than 10nm) have demonstrated that the HD PFS can effectively neutralise wafer charging with a large operation window in beam current, arc current and tube bias voltage. All the advanced antenna MOS capacitors for these tests were supplied by Matsushita Electronics Corp.

The yield of a test matrix of the MOS capacitors with 1E6 antennas and the gate oxide thickness with 5nm on a p-substrate is plotted in Fig.6. The implant was

As<sup>+</sup>/20keV/10mA/5E15 cm<sup>-2</sup>. The yield was 100% with 0V of tube bias and at arc currents of 0.5, 1 and 2A. The yield was also 100% with 1A of arc current and at tube bias of 0, -10 and -20V.

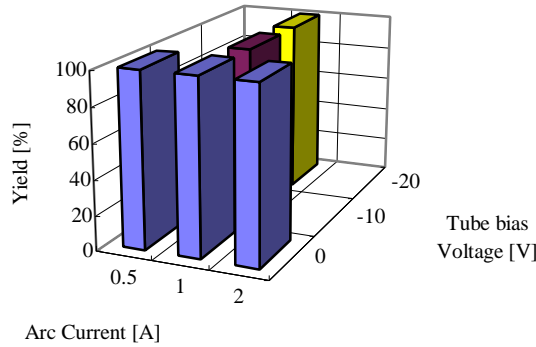


Fig.6. Yield of MOS capacitors (1E6 antenna ratio and 5nm gate oxide) is plotted against arc current and tube bias voltage. The implant was As<sup>+</sup>/20keV/10mA/5E15 cm<sup>-2</sup>.

In comparison, the same implant with the Previous PFS gave a yield of less than 60% for 1E6 antennas with 4A of arc when the tube bias was -10V and -20V.

A result of the HD PFS and Previous PFS is plotted in Fig.7 for the MOS capacitors at antenna ratios of 3.2E4, 1E5, 3.2E5 and 1E6 with 5nm gate oxide on n-substrate. In general, antenna MOS capacitor fabricated on n-substrate is more sensitive for negative charging damage than the one on p-substrate. The test was done with no beam at a typical operation to see the negative charging breakdown due to high energy electrons. HD PFS at 1A of arc and the previous PFS at 4A of arc. Yield of HD PFS was 100% for all devices. On the other hand, the yield of the previous PFS dropped to 20% for the 1E6 antenna. The previous PFS caused negative charging breakdown under the no beam condition. This is an evidence that high energy electrons can reach the wafers with the previous PFS when the tube bias is used. From these results, it is clear that the net electron energy of HD PFS is significantly reduced. Cusp magnets on the guide tube appear to provide the “energy filter” effect which prevents high energy secondary electrons from reaching the wafer surface.

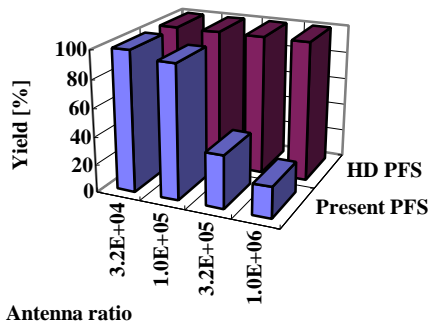


Fig.7. Yield of the HD PFS and Solenoid PFS with no beam are plotted for antenna ratios of 3.2E4, 1E5, 3.2E5 and 1E6 at 5nm gate oxide.

Fig.8-1,2,3 and 4 show the breakdown frequency of the antenna MOS capacitors at different gate oxide thickness (10nm, 7.5nm, 5nm and 3.5nm). Data indicate a dependence of the damage on electron energy and the two major device parameters i.e. antenna ratio and oxide thickness [7, 8]. Change in electron energy means a difference in flux ratio between primary electrons from the

arc chamber (low energy electrons) and secondary electrons produced along the beamline (higher energy electrons).

Fig.8-1 and 2 show that HD PFS can hardly cause any damage for the devices of 7.5nm gate oxide or thicker unless the electron energy is deliberately increased. As the gate oxide becomes thinner, the breakdown frequency increased as shown in Fig.8-3 and 4. However, even with the extremely charge sensitive devices such as 3.5nm gate oxide and 1E6 antenna ratio, HD PFS can still achieve perfect yield by controlling the electron energy to the lower end.

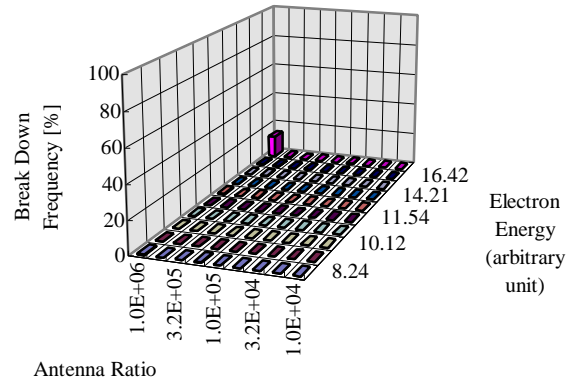


Fig.8-1. Yield versus Electron energy versus Antenna Ratio with 10nm gate oxide MOS capacitors. The implant was As<sup>+</sup>/20keV/10mA/5E15 cm<sup>-2</sup>.

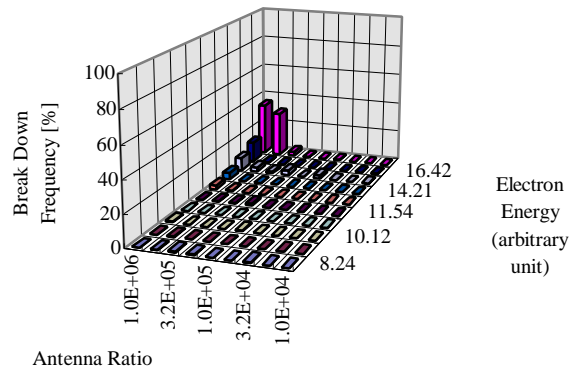


Fig.8-2. Yield versus Electron energy versus Antenna Ratio with 7.5nm gate oxide MOS capacitors. The implant was As<sup>+</sup>/20keV/10mA/5E15 cm<sup>-2</sup>.

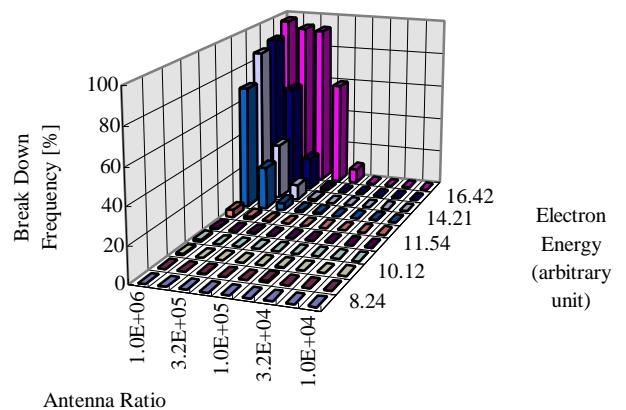


Fig.8-3. Yield versus Electron energy versus Antenna Ratio with 5nm gate oxide MOS capacitors. The implant was As<sup>+</sup>/20keV/10mA/5E15 cm<sup>-2</sup>.

The yield of MOS capacitors on p-substrate at a typical operating condition of HD PFS, 1A of arc and 0V of guide

tube, are plotted in Fig.9 for different antenna ratio and gate oxide thickness. The implant condition was  $As^+/20keV/10mA/5E15\text{ cm}^{-2}$ . The yield was 100% on all cases (antenna ratio at  $1E5$  and  $1E6$ , gate thickness at 10nm, 5nm and 3.5nm). This is a clear indication that HD PFS has a large enough window to cover from the present technology (devices of 10nm gate) to the future requirement (devices of 3.5nm gate) [10].

### Flood Gun (9200EFG)

EEPROM Vt Shift (Ave. = -0.06V, sigma = 1.89)  
 $As^+/40keV/12mA/4E15$   
 Floodgun (emission 40mA)

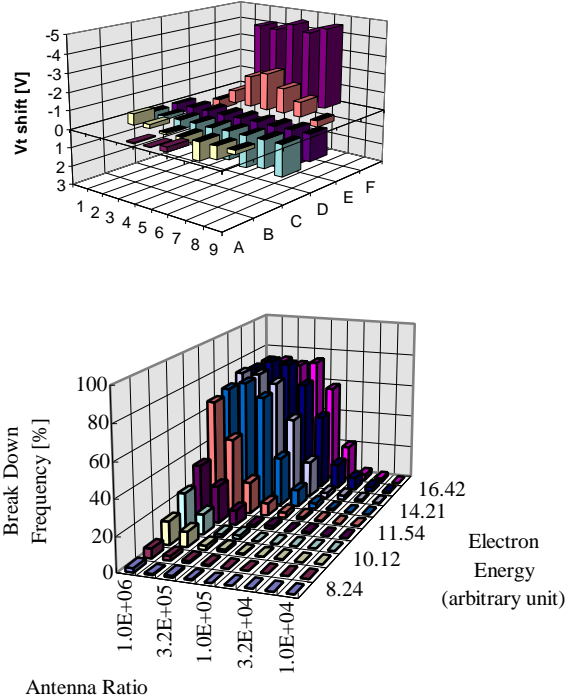


Fig.8-4. Yield versus Electron energy versus Antenna Ratio with 3.5nm gate oxide MOS capacitors. The implant was  $As^+/20keV/10mA/5E15\text{ cm}^{-2}$ .

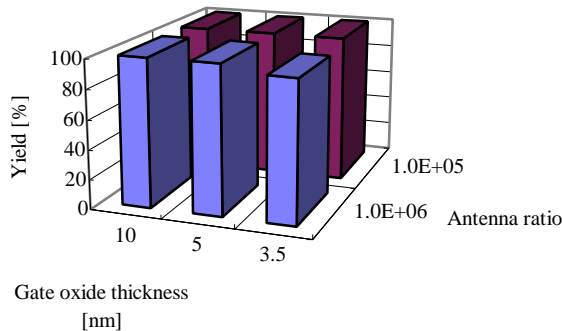


Fig.9. The yield of MOS capacitors at a typical operating condition of HD PFS. The implant was  $As^+/20keV/10mA/5E15\text{ cm}^{-2}$ . HD PFS was operated at 1A of arc and 0V of guide tube, with 1.4 sccm argon.

### E. EEPROM

HD PFS demonstrated a precise Vt control with remarkable uniformity across the wafer. The results are shown in Figs.5-1 and 2.

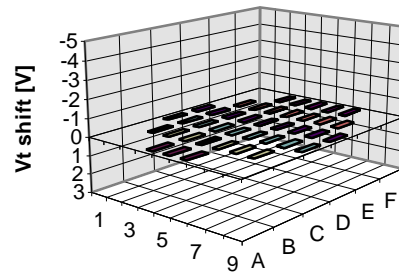


Fig.5-1 Vt shift on EEPROM. Implant condition :  $As^+/40keV/12mA/4E15\text{ cm}^{-2}$ . HD PFS : 0.5A/-10V. Average Vt shift : 0.00V. Sigma : 0.01V. [9]

### . CONCLUSION

HD PFS has been developed for Applied Materials ion implanters in order to achieve an ideal charging control for 0.15um technology and beyond. The system offers an ample supply (150mA at 1A or arc) of low energy electrons (<3eV), that can neutralise the positive charging induced by ion beams while demonstrating the minimum risk of negative charging. The system has shown the perfect yield over a wide range of operation window by using Matsushita's advanced MOS capacitor devices with antenna ratios from  $3.2E4$  to  $1E6$  and gate oxide thickness from 3.5nm to 10nm [10].

Low arc operation also prolongs the source life (> 6 months proven) and reduces tungsten contamination (<  $1E10\text{ cm}^{-2}$ ).

Fig.5-2 Vt shift on EEPROM. Implant condition :  $As^+/40keV/12mA/4E15\text{ cm}^{-2}$ . Floodgun : 40mA. Average Vt shift : -0.06V. Sigma : 1.89V.

### . ACKNOWLEDGEMENT

The authors would like to thank Mr.Masanori Takahashi and Mr.Yasuhiro Hori for their valued contribution in planning and completing the evaluation of HD PFS.

### REFERENCES

- [1] D.Aitken, in Ion Implantation Techniques, edited by H.Ryssel and H.Glawischnig, Springer, 351 (1982)
- [2] M.E.Mack, in Handbook of Ion Implantation Technology, edited by J.F.Ziegler, Elsevier, 599 (1992)
- [3] H.Ito, T.Kamata, J.England, I.Fotheringham, F.Plumb and M.I.Current, Nucl. Instr. And Meth. B 96 (1995) 30-33
- [4] H.Ito and M.I.Current, Plasma Flood System - Physics of Low Energy Electron Generation, Plasma Coupling, Electron Transport and Surface Charge Neutralisation, Ion Implantation Technology Conference Proceeding, pp.432-435 (1996)

- [5] M.C.Vella, N.Aoki, H.Ito, H.Asechi, P.Hacker, R.Couchot, S.Nishio, M.Reilly and N.Sugiyama, Plasma Flood System for the Precision Implant 9200, Ion Implantation Technology Conference Proceeding, pp.428-431 (1996)
- [6] M.I.Current, M.C.Vella and W.Lukaszek, Ion Implantation Technology Conference Proceeding, pp.53-56 (1996)
- [7] D.L.Smatlak, M.E.Mack and S.Metha, Nucl. Instr and Meth. B 96 (1995) 22-29.
- [8] M.E.Mack, Handbook of Ion Implantation Technology, J.F.Ziegler(Ed), North-Holland (1992)
- [9] M.C.Vella, W.Lukaszek, M.I.Current and N.H.Tripsas, Nucl. Instr and Meth. B 96 (1995) 48-51.
- [10] M.Niwayama, H.Kubo, K.Yoneda, H.Asechi and H.Ito, these proceedings.